Amendments to the Claims

1. (currently amended) A method of communicating with a mass storage device, comprising:

receiving ATA/ATAPI signals from a mass storage device into a bridging circuit;

updating a state machine in response to embedded commands in the ATA/ATAPI signals;

converting the ATA/ATAPI signals from the mass storage device into USB signals using the bridging circuit in response to the state machine; and

outputting the USB signals from the bridging circuit.

2. (currently amended) A method according to claim 1, wherein the bridging circuit is provided in a single, bridging chip, the bridging chip including:

a USB physical interface transceiver;

a serial interface engine coupled to the USB physical interface transceiver;

an input/output interface coupled to the serial interface engine;

a ram control circuit coupled to the input/output interface;

a global control circuit coupled to the input/output interface;

a translate circuit coupled to the global control circuit; and

a disk interface coupled to the ram control circuit and the translate circuit.

3. (original) A method according to claim 1, wherein the bridging circuit is provided on a motherboard of the mass storage device.

4. (original) A method according to claim 1, wherein the bridging circuit is provided on a secondary board.

5. (currently amended) A method according to claim 4, wherein a mass storage device motherboard outputs the ATA/ATAPI signals, and wherein the secondary board receives the

ATA/ATAPI signals from the mass storage device motherboard and converts them into USB signals.

6. (currently amended) A motherboard for a mass storage device, said motherboard comprising:

input logic configured to receive an input signal from a read unit of the mass storage device;

a bridging circuit configured to receive the input signal from the input logic and convert the input signal into a USB signal, the bridging circuit including:

a USB physical interface transceiver;

a serial interface engine coupled to the USB physical interface transceiver;

an input/output interface coupled to the serial interface engine;

a ram control circuit coupled to the input/output interface;

a global control circuit coupled to the input/output interface;

a translate circuit coupled to the global control circuit; and

a disk interface coupled to the ram control circuit and the translate circuit; and

output circuitry configured to output the USB signal from the motherboard.

7. (original) A mass storage device motherboard according to claim 6, wherein the bridging circuit comprises a bridging chip for converting the input signal into the USB signal.

8. (currently amended) A mass storage device motherboard according to claim 7 ~~6~~, wherein the bridging chip comprises:

an ATA/ATAPI interface configured to receive a ATA/ATAPI signal ~~signals~~ from the input logic; and

a state machine configured to translate the ATA/ATAPI signals into the USB signal;

wherein:

the [[a]] disk interface is configured to receive the ATA/ATAPI signals from the ATA/ATAPI interface;

~~a serial interface engine; and~~

the [[a]] USB physical interface transceiver is configured to receive signals from the serial interface engine and output USB signals to a USB interface;

the state machine is updated in response to embedded commands in the ATA/ATAPI signals.

9. (currently amended) A secondary board configured to enable communication between a mass storage device motherboard and a host motherboard, said secondary board comprising:

a connector port for receiving signals from the mass storage device motherboard;

a bridging circuit for converting the signals from the mass storage device motherboard into USB signals, the bridging circuit including:

a USB physical interface transceiver;

a serial interface engine coupled to the USB physical interface transceiver;

an input/output interface coupled to the serial interface engine;

a ram control circuit coupled to the input/output interface;

a global control circuit coupled to the input/output interface;

a translate circuit coupled to the global control circuit; and

a disk interface coupled to the ram control circuit and the translate circuit; and

a USB connector port for outputting the USB signals to the host motherboard.

10. (currently amended) A secondary board according to claim 9, wherein the bridging circuit comprises a bridging chip configured to translate the signals from the mass storage device motherboard into the USB signals.

11. (cancelled)

12. (currently amended) A secondary board according to claim 10 ~~11~~, wherein:

the bridging circuit includes a state machine responsive to embedded commands in the ATA/ATAPI signals configured to translate the signals from the mass storage device motherboard into the USB signals;

the disk interface receives ATA/ATAPI signals through an ATA/ATAPI interface, and

~~wherein~~

the bridging circuit is configured to translate the ATA/ATAPI signals ~~are converted~~ into USB 2.0 signals in response to the state machine and ~~are~~ output the USB 2.0 signals to a USB Interface through the USB physical interface transceiver.

13. (currently amended) A bridging chip comprising:

an input configured to receive ATA/ATAPI signals;

a USB physical interface transceiver;

conversion logic configured to convert the ATA/ATAPI signals into USB signals, the conversion logic including:

a serial interface engine coupled to the USB physical interface transceiver;

an input/output interface coupled to the serial interface engine;

a ram control circuit coupled to the input/output interface;

a global control circuit coupled to the input/output interface;

a translate circuit coupled to the global control circuit; and

a disk interface coupled to the input, the ram control circuit, and the translate circuit; and

an output coupled to the USB physical interface transceiver and configured to output the USB signals.

14. (currently amended) A chip according to claim 13,wherein the conversion logic includes a state machine responsive to embedded commands in the ATA/ATAPI signals ~~said input comprises an ATA/ATAPI interface arranged to receive the ATA/ATAPI signals and a disk interface configured to receive ATA/ATAPI signals from the ATA/ATAPI interface; wherein said conversion logic comprises a serial interface engine and a USB physical interface transceiver, said interface transceiver being configured to receive signals from the serial interface engine and output USB signals to a USB interface~~.

15. (original) A chip according to claim 13, wherein the chip is located on a mass storage device motherboard.

16. (original) A chip according to claim 13, wherein the chip is located on a secondary board.

17. (original) A chip according to claim 16, wherein the secondary board is arranged to receive ATA/ATAPI signals from a motherboard of the mass storage device.

18. (currently amended) A method of converting signals from a mass storage device into USB signals, said method comprising:

receiving a signal from a mass storage device into a bridging chip, the bridging chip including:

a USB physical interface transceiver;

a serial interface engine coupled to the USB physical interface transceiver;

an input/output interface coupled to the serial interface engine;

a ram control circuit coupled to the input/output interface;

a global control circuit coupled to the input/output interface;

a translate circuit coupled to the global control circuit; and

a disk interface coupled to the ram control circuit and the translate circuit;

updating a state machine in the bridging chip in response to embedded commands in the signal from the mass storage device;

converting the signal from the mass storage device into a USB signal in response to the state machine; and

outputting the USB signal from the bridging chip.

19. (original) A method of converting signals according to claim 18, wherein said bridging chip is located on a motherboard of the mass storage device.

20. (original) A method of converting signals according to claim 18, wherein the bridging chip is located on a secondary board arranged in communication with a motherboard of the mass storage device.